What is claimed is:

1. A flat panel display, comprising:

a power unit for supplying constant voltage to each unit;

a gate voltage generating unit for generating a gate on/off voltage;;

a controller for generating a scan control signal and a column control signal by utilizing driving data and a driving control signal, controlling and outputting timing format of R, G, B data, and generating gamma data having a plurality of values for gradation;

a scan driver unit for outputting a scan signal utilizing the scan control signal and said gate on/off voltage;

a column driver unit for converting the gamma data into an analog gradation voltage, and outputting a column signal utilizing the column control signal , R, G, B data and the gradation voltage; and

a flat display panel for displaying a predetermined image by utilizing the scan signal and the column signal.

2. A flat panel display according to claim 1, wherein said controller transmits R, G, B data of a plurality of bits and gamma data of a plurality of bits to said column driver unit through different transmission line.

3. A flat panel display according to claim 2, wherein said column driver unit comprises a plurality of column driver ICs, each of the column driver ICs comprising:

a first memory for storing the gamma data;

a first decoder for decoding the gamma data stored in said first memory;

a first A/D converter for converting the decoded gamma data into an analog

gradation voltage and outputting the converted analog gradation voltage;

a first shift register for sequentially shifting output in correspondence to a column line;

a first data latch for storing in column line unit data of corresponding capacity from among R, G, B data in accordance with the output of said first shift register;

a second D/A converter for selecting and outputting gradation voltage corresponding to data value supplied from said first data latch; and

a first buffer for buffering the gradation voltage output from said second D/A converter, and outputting a column signal in line units.

4. A flat panel display according to claim 1, wherein said controller further comprises:

a signal processing unit for controlling timing format of R, G, B data by utilizing driving data and a driving control signal, outputting the controlled result, and generating and outputting a scan control signal and a column control signal;

a gamma data generating unit for generating a plurality of data for gradation with reference to the constant voltage supplied from said power unit and outputting gamma data; and

a mixer unit for mixing the gamma data to a blanking section of the R, G, B data and outputting the mixed result,

wherein the R, G, B data and the gamma data are transmitted through an identical line.

5. A flat panel display according to claim 4, wherein said column driver unit is constituted by a plurality of column driver ICs, each of the column driver ICs

comprising;

a data diving unit for dividing the R, G, B data and the gamma data;

a second memory for storing the gamma data divided by said data diving unit;

a second decoder for decoding gamma data of said second memory;

a third D/A converter for converting the decoded gamma data into an analog gradation voltage and outputting the converted voltage;

a second shift register for sequentially shifting output corresponding to column line;

a second data latch for storing data of corresponding capacity from among R, G, B data according to an output of said second shift register;

a fourth D/A converter for selecting gradation voltage corresponding to value of data supplied from said second data latch and outputting selected gradation voltage; and

a second buffer for buffering the gradation voltage output from said fourth D/A converter and outputting a column signal in line units.

6. A flat panel display, comprising:

a power unit for supplying a constant voltage;

a gate voltage generating unit for generating a gate on/off voltage;

a controller for generating a scan control signal and a column control signal by utilizing driving data and a driving control signal, controlling and outputting timing format of R, G, B data, generating gamma data having a plurality of values for gradation with reference to the constant voltage supplied from said power unit, and encoding and outputting in differential signal the scan control signal, column control signal, R, G, B

data;

a scan driver unit for decoding the scan control signal included in the differential signal and outputting a scan signal utilizing the scan control signal and the gate on/off voltage;

a column driver unit for decoding the column control signal, R, G, B data and column data included in the differential signal, converting the gamma data into an analog gradation voltage, and outputting a column signal utilizing the column control signal , R, G, B data and the gradation voltage; and

a flat display panel for displaying a predetermined image by utilizing the scan signal and the column signal.

7. A flat panel display according to claim 6, wherein said controller comprises:

a first signal processing unit for controlling timing format of R, G, B data by utilizing the driving data and the driving control signal, outputting the controlled result, and generating and outputting the scan control signal and the column control signal;

a gamma data generating unit for generating plural data for gradation with reference to the constant voltage supplied from said power unit and outputting gamma data; and

a differential signal transmitting unit for encoding into differential signal the scan control signal, column control signal, R, G, B data and gamma data, and transmitting the result.

8. A flat panel display according to claim 7, wherein said column driver unit comprises a plurality of column driver ICs, each of the column driver ICs comprising;

a differential signal receiving unit for decoding the differential signal;

a memory for storing the decoded column control signal, R, G, B data and gamma data;

a decoder for decoding the gamma data stored in said memory;

a first A/D converter for converting the decoded gamma data into an analog gradation voltage and outputting the converted analog gradation voltage;

a shift register for sequentially shifting output corresponding to a column line;

a data latch for storing in column line unit data of corresponding capacity from among R, G, B data according to the output of said shift register;

a second D/A converter for selecting and outputting gradation voltage corresponding to data value supplied from said data latch; and

a buffer for buffering said gradation voltage output from said second D/A converter, and outputting a column signal in line units.

9. A flat panel display according to claim 6, wherein said differential signal is an RSDS signal.

10. A flat panel display according to claim 6, wherein said differential signal is an LVDS signal.

11. A flat panel display according to claim 6, wherein said differential signal is a TMDS signal.

12. A flat panel display according to claim 7, wherein said differential signal is an RSDS signal.

13. A flat panel display according to claim 7, wherein said differential signal

is an LVDS signal.

14. A flat panel display according to claim 7, wherein said differential signal is a TMDS signal.

15. A flat panel display according to claim 8, wherein said differential signal is an RSDS signal.

16. A flat panel display according to claim 8, wherein said differential signal is an LVDS signal.

17. A flat panel display according to claim 8, wherein said differential signal is a TMDS signal.